Parallel Input (635-0751-001, -002)

Rockwell International

instructions

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1. DESCRIPTION

Parallel Input 635-0751-001, -002, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

2. PRINCIPLES OF OPERATION

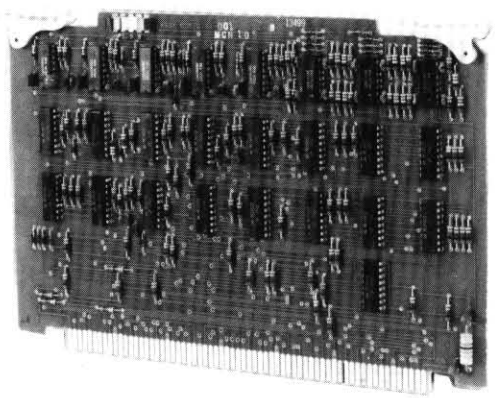
2.1 General

The parallel input card consists of two primary circuits: sixteen 8-channel multiplexers, and five gate generators. Each multiplexer receives up to eight inputs developed by the unit front panel controls. Address bits, from the serial interface card, select individual inputs for transfer to the single output from the multiplexer. These address bits are developed from word gate signals produced by the gate generator circuits.

2.2 Multiplexers

The multiplexers are integrated circuits functioning as 8-channel data selectors. (Refer to figure 2 for a block diagram and truth table of the component.) Note, from reference to the schematic diagram, figure 5, that the circuit arrangement is two sections of eight multiplexers each. The MX8 input selects the active section. When at a logic 1 level, the disable input of the multiplexer keeps the output at a high impedance. A logic 0 input allows the output to be developed from the eight input lines. Inverter U10F keeps one section disabled while the other is enabled.

The MX1, MX2, and MX4 inputs, applied simultaneously to all multiplexers, controls which of the eight input signals to each multiplexer is coupled to the output line. (Refer to the truth table of figure 2.) The resulting output signals from the eight multiplexers are eight data bits of the control word for

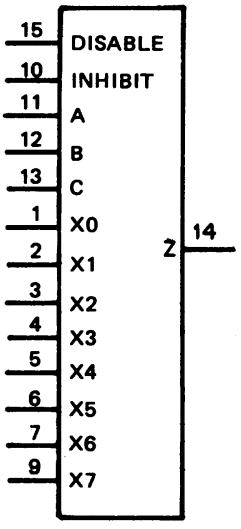


TP5-2312-017

Parallel Input
Figure 1

NOTICE: This section replaces first edition dated 1 June 1977.

BLOCK DIAGRAM



TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	HIGH IMPEDANCE

X = DON'T CARE

TP5-2026-011

8-Channel Data Selector MC14512
Figure 2

the unit under control. These data bits are coupled to the serial interface card for parallel-to-serial conversion, word formation, and application to the control bus.

2.3 Gate Generators

When a front panel control is switched to a different position, a gate signal is developed by one of five gate generators. Each of these generator circuits is two multivibrators that develop a single output pulse. The output is a word or address gate signal applied to the serial interface card.

The two multivibrators are connected in series. (Refer to the schematic diagram, figure 5.) An input pulse to the first multivibrator causes an output pulse from that multivibrator of about 0.1 second width.

The output pulse from the first multivibrator is the input to the second multivibrator. The second circuit does not trigger until the end (1-to-0 transition) of the first output pulse. This delay gives time for switch settling into the final position selected.

The output from the second multivibrator is a 0.1-millisecond pulse for the word gates and a 10-microsecond pulse for the address gate. Figure 3 shows a block diagram and timing waveforms for the multivibrators used in the word and address gate generator circuits.

3. TESTING/TROUBLESHOOTING PROCEDURES

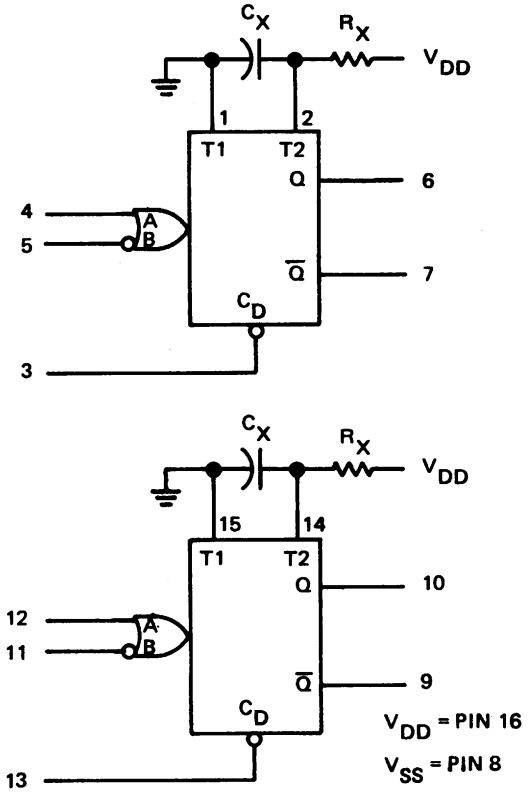
3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel input are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the parallel input. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

BLOCK DIAGRAM

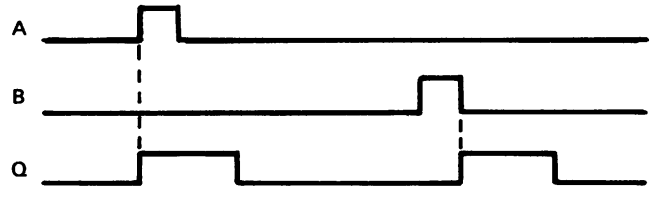


A INPUT TERMINAL CLOCKS ON 0-TO-1 TRANSITION.

B INPUT TERMINAL CLOCKS ON 1-TO-0 TRANSITION.

C_D (RESET) TERMINAL, WHEN SWITCHED TO LOGIC 0, IMMEDIATELY TERMINATES OUTPUT PULSE.

R_X AND C_X ARE EXTERNAL COMPONENTS.



TP5-2299-011

Dual Monostable Multivibrator CD4098BE
Figure 3

Table 1. Parallel Input, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel input in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		
	a. Remove top cover of unit containing parallel input to be tested.		
	b. Remove parallel input. Install it on an extender card and place it in the control unit.		
	c. Set control unit and local unit LINE SELECTOR switches to 115 V.		
	d. Connect control unit and local unit to 115-V ac power source and set power on.		
	e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45	+15 ±1.0 V dc.	
	P1-65	+5 ±0.5 V dc.	
	P1-114	-15 ±1.0 V dc.	
	f. Strap local unit for address 0.		
	g. Connect local unit to control unit.		
2. Word and address gates	a. Connect oscilloscope to TP2 (red).		
	b. Set control unit KEY switch to LOCK and note oscilloscope.	A logic level 1, 100-µs (nominal) pulse.	Check U2A, U2B, and associated circuit.
	c. Set control unit KEY switch to NORM and note oscilloscope.	Same as step b.	Same as step b.
	d. Connect oscilloscope to TP3 (orange).		
	e. Set control unit PA PWR switch to STBY and note oscilloscope.	A logic level 1, 100-µs (nominal) pulse.	Check U3A, U3B, and associated circuit.
	f. Set control unit PA PWR switch to OFF and note oscilloscope.	Same as step e.	Same as step e.
(Cont)	g. Connect oscilloscope to TP4 (yellow).		

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Word and address gates (Cont)	h. Rotate each control unit FREQUENCY KHZ thumb wheel and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U1A, U1B, and associated circuit.
	i. Connect oscilloscope to TP5 (green).		
	j. Set control unit MODE switch to each mode position and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U5A, U5B, and associated circuit.
	k. Connect oscilloscope to P1-88.		
	l. Rotate control unit ADDRESS switch and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U4A, U4B, and associated circuit.
	m. Connect +5-V dc input to P1-66.		
	n. Check voltage levels at:		
	TP2	NLT +4.0 V dc.	Check CR1.
	TP3	NLT +4.0 V dc.	Check CR2.
	TP4	NLT +4.0 V dc.	Check CR4.
	TP5	NLT +4.0 V dc.	Check CR3.
	o. Remove +5 V dc from P1-66.		

Note

Tests 3 through 18 are output tests. During all of these tests serial interface card A13 is removed from unit under test and mux inputs are strapped according to word and character being tested. To strap a logic 1 input, connect a 4700-Ω resistor in series between the mux input pin and +5 V dc. To strap a logic 0 input, connect directly from the mux input pin to ground. See following chart and figure for mux input/output strapping and setup requirements. Where front-panel controls are shown, these controls may be used to apply the appropriate inputs. If they are not used their associated front-panel connector must be disconnected.

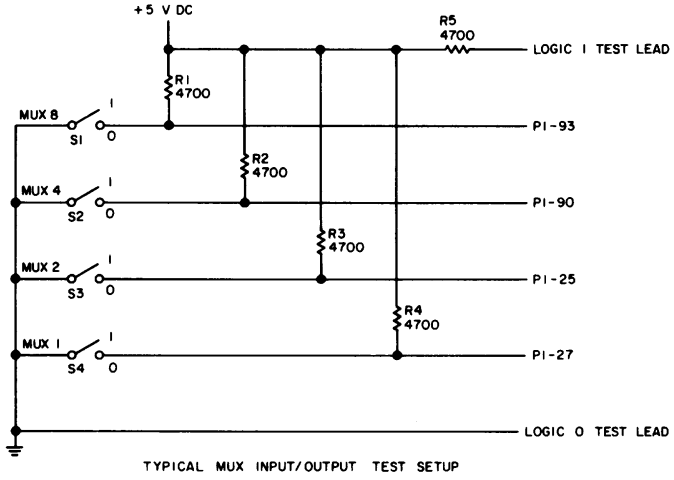
MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD								
				WORD NO	CHARACTER NO	OUTPUT BIT NO						
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	0	0	0	1	2	P1-62	P1-127	P1-63	P1-128	P1-64	P1-129	P1-38	P1-103
0	0	0	1	1	3	P1-58	P1-123	P1-59	P1-124	P1-60	P1-125	P1-61	P1-126
0	0	1	0	1	4	P1-54	P1-119	P1-55	P1-120	P1-56	P1-121	P1-57	P1-122
0	0	1	1	1	5	P1-50	P1-115	P1-51	P1-116	P1-52	P1-117	P1-53	P1-118
0	1	0	0	2	2	P1-87	P1-10	P1-75	P1-11	P1-76	NA	NA	NA
0	1	0	1	2	3	P1-20	P1-19	P1-85	P1-84	P1-37	P1-106	P1-41	NA

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD								
				WORD NO	CHARACTER NO	OUTPUT BIT NO						
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	1	1	0	2	4	P1-32	P1-97	P1-33	P1-98	P1-34	P1-35	P1-99	P1-100
0	1	1	1	2	5	P1-21	P1-91	P1-92	P1-74	P1-9	P1-72	P1-8	P1-73
1	0	0	0	3	2	P1-112	P1-47	P1-113	P1-48	P1-107	NA	NA	NA
1	0	0	1	3	3	P1-42	P1-108	P1-43	P1-109	P1-44	P1-110	P1-111	P1-46
1	0	1	0	3	4	NA	NA	NA	NA	NA	NA	NA	NA
1	0	1	1	3	5	P1-79	P1-14	P1-78	P1-82	P1-81	NA	NA	NA
1	1	0	0	4	2	NA	NA	NA	NA	P1-68	NA	NA	NA
1	1	0	1	4	3	P1-18	P1-101	P1-39	P1-83	P1-36	P1-105	P1-40	P1-2
1	1	1	0	4	4	P1-3	P1-86	P1-49	P1-67	P1-70	P1-5	P1-4	P1-69
1	1	1	1	4	5	P1-80	P1-16	P1-95	P1-71	NA	NA	NA	NA

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.



TYPICAL MUX INPUT/OUTPUT TEST SETUP

TP5-4247-013

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. Word 1, character 2 outputs</td><td>a. Strap mux control lines for word 1, character 2.

b. Apply logic 1 inputs at inputs associated with word 1, character 2 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 2 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>1 MHz 1</td><td>1</td><td>62</td><td>26</td><td>U25, U18</td></tr>
<tr><td>1 MHz 2</td><td>2</td><td>127</td><td>28</td><td>U15, U19</td></tr>
<tr><td>1 MHz 4</td><td>3</td><td>63</td><td>29</td><td>U23, U20</td></tr>
<tr><td>1 MHz 8</td><td>4</td><td>128</td><td>94</td><td>U21, U17</td></tr>
<tr><td>10 MHz 1</td><td>5</td><td>64</td><td>30</td><td>U24, U11</td></tr>
<tr><td>10 MHz 2</td><td>6</td><td>129</td><td>31</td><td>U16, U13</td></tr>
<tr><td>NA</td><td>7</td><td>38</td><td>96</td><td>U22, U12</td></tr>
<tr><td>NA</td><td>8</td><td>103</td><td>104</td><td>U14, R42, U9</td></tr>
</table>
</td></tr>
<tr><td>4. Word 1, character 3 outputs

(Cont)</td><td>a. Strap mux control lines for word 1, character 3.

b. Apply logic 1 inputs at inputs associated with word 1, character 3 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 3 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. Word 1, character 3 outputs (Cont)</td><td>
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>10 kHz 1</td><td>1</td><td>58</td><td>26</td><td>U25, U18</td></tr>
<tr><td>10 kHz 2</td><td>2</td><td>123</td><td>28</td><td>U15, U19</td></tr>
<tr><td>10 kHz 4</td><td>3</td><td>59</td><td>29</td><td>U23, U20</td></tr>
<tr><td>10 kHz 8</td><td>4</td><td>124</td><td>94</td><td>U21, U17</td></tr>
<tr><td>100 kHz 1</td><td>5</td><td>60</td><td>30</td><td>U24, U11</td></tr>
<tr><td>100 kHz 2</td><td>6</td><td>125</td><td>31</td><td>U16, U13</td></tr>
<tr><td>100 kHz 4</td><td>7</td><td>61</td><td>96</td><td>U22, U12</td></tr>
<tr><td>100 kHz 8</td><td>8</td><td>126</td><td>104</td><td>U14, U9</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>5. Word 1, character 4 outputs</td><td>a. Strap mux control lines for word 1, character 4.

b. Apply logic 1 inputs at inputs associated with word 1, character 4 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 4 (see chart).</td><td>Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td></td><td colspan="3">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>100 Hz 1</td><td>1</td><td>54</td><td>26</td><td>U25, U18</td></tr>
<tr><td>100 Hz 2</td><td>2</td><td>119</td><td>28</td><td>U15, U19</td></tr>
<tr><td>100 Hz 4</td><td>3</td><td>55</td><td>29</td><td>U23, U20</td></tr>
<tr><td>100 Hz 8</td><td>4</td><td>120</td><td>94</td><td>U21, U17</td></tr>
<tr><td>1 kHz 1</td><td>5</td><td>56</td><td>30</td><td>U24, U11</td></tr>
<tr><td>1 kHz 2</td><td>6</td><td>121</td><td>31</td><td>U16, U13</td></tr>
<tr><td>1 kHz 4</td><td>7</td><td>57</td><td>96</td><td>U22, U12</td></tr>
<tr><td>1 kHz 8</td><td>8</td><td>122</td><td>104</td><td>U14, U9</td></tr>
</table>
</td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>6. Word 1, character 5 outputs</td><td>a. Strap mux control lines for word 1, character 5.

b. Apply logic 1 inputs at inputs associated with word 1, character 5 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 5 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>50</td><td>26</td><td>U25, R68, U18</td></tr>
<tr><td>NA</td><td>2</td><td>115</td><td>28</td><td>U15, R64, U19</td></tr>
<tr><td>NA</td><td>3</td><td>51</td><td>29</td><td>U23, R60, U20</td></tr>
<tr><td>NA</td><td>4</td><td>116</td><td>94</td><td>U21, R56, U17</td></tr>
<tr><td>*10 Hz 1</td><td>5</td><td>52</td><td>30</td><td>U24, R52, U11</td></tr>
<tr><td>*10 Hz 2</td><td>6</td><td>117</td><td>31</td><td>U16, R49, U13</td></tr>
<tr><td>*10 Hz 4</td><td>7</td><td>53</td><td>96</td><td>U22, R46, U12</td></tr>
<tr><td>*10 Hz 8</td><td>8</td><td>118</td><td>104</td><td>U14, R43, U9</td></tr>
<tr><td colspan="5">*Applicable only with 10-Hz front-panel tuning.</td></tr>
</table>
</td></tr>
<tr><td>7. Word 2, character 2 outputs

(Cont)</td><td>a. Strap mux control lines for word 2, character 2.

b. Apply logic 1 inputs at inputs associated with word 2, character 2 (see chart).</td><td>Note

Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>7. Word 2, character 2 outputs (Cont)</td><td>Note
RF GAIN switch applies logic 1 input in the position indicated in the chart (positions read as MAX minus X number of positions). In the MAX position, this switch applies logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 2, character 2 (see chart).</td><td>Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>87</td><td>26</td><td>U25, R69, U18</td></tr>
<tr><td>RF GAIN MAX-1</td><td>2</td><td>10</td><td>28</td><td>U15, R65, U19</td></tr>
<tr><td>RF GAIN MAX-2</td><td>3</td><td>75</td><td>29</td><td>U23, R61, U20</td></tr>
<tr><td>RF GAIN MAX-4</td><td>4</td><td>11</td><td>94</td><td>U21, R57, U17</td></tr>
<tr><td>RF GAIN MAX-8</td><td>5</td><td>76</td><td>30</td><td>U24, R53, U11</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U16, U13</td></tr>
<tr><td>NA</td><td>7</td><td>38</td><td>96</td><td>U22, U12</td></tr>
<tr><td>NA</td><td>8</td><td>103</td><td>104</td><td>U14, R42, U9</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>8. Word 2, character 3 outputs

(Cont)</td><td>a. Strap mux control lines for word 2, character 3.

b. Apply logic 1 inputs at inputs associated with word 2, character 3 (see chart).

Note
AGC switch applies logic 1 input in the position indicated in the chart. In the AGC-SLOW position, this switch applies logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 2, character 3 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that associated ouputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

8. Word 2, character 3 outputs (Cont)

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
AGC-FAST (B)	1	20	26	U25, U18
AGC-OFF (B)	2	19	28	U15, U19
AGC-FAST (A)	3	85	29	U23, U20
AGC-OFF (A)	4	84	94	U21, U17
NA	5	37	30	U24, U11
NA	6	106	31	U16, U13
NA	7	41	96	U22, U12
NA	8	*	104	U14, U9

*Grounded input.

9. Word 2, character 4 outputs

a. Strap mux control lines for word 2, character 4.

b. Apply logic 1 inputs at inputs associated with word 2, character 4 (see chart).

Verify that associated outputs are at logic 1.

Note

MODE switch and/or BANDWIDTH switch applies logic 1 input in the position indicated in the chart. In the ISB position, the MODE switch applies logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 2, character 4 (see chart).

Verify that associated outputs are at logic 0.

FRONT-PANEL CONTROL (MODE)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
SSB/CW-USB or USB	1	32	26	U25, R70, U18
SSB/CW-LSB or LSB	2	97	28	U15, R66, U19
*SSB/CW-A	3	33	29	U23, R62, U20
*SSB/CW-B	4	98	94	U21, R58, U17
*SSB/CW-C	5	34	30	U24, R54, U11
*SSB/CW-D	6	35	31	U16, R50, U13
*SSB/CW-E	7	99	96	U22, R47, U12
*SSB/CW-16	8	100	104	U14, R44, U9

*SSB/CW applicable only on receiver control.

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>10. Word 2, character 5 outputs</td><td>a. Strap mux control lines for word 2, character 5.

b. Apply logic 1 inputs at inputs associated with word 2, character 5 (see chart).

Note

MODE switch applies logic 1 input in the position indicated in the chart. In any other position, the MODE switch applies logic 0 input.

c. Apply logic 0 inputs at inputs associated with word 2, character 5 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL (MODE)</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>21</td><td>26</td><td>U25, R71, U18</td></tr>
<tr><td>NA</td><td>2</td><td>91</td><td>28</td><td>U15, R67, U19</td></tr>
<tr><td>NA</td><td>3</td><td>92</td><td>29</td><td>U23, R63, U20</td></tr>
<tr><td>ISB</td><td>4</td><td>74</td><td>94</td><td>U21, R59, U17</td></tr>
<tr><td>*CW</td><td>5</td><td>9</td><td>30</td><td>U24, R55, U11</td></tr>
<tr><td>CW, LSB, USB, ISB, or SSB/CW</td><td>6</td><td>72</td><td>31</td><td>U16, R51, U13</td></tr>
<tr><td>AM</td><td>7</td><td>8</td><td>96</td><td>U22, R48, U12</td></tr>
<tr><td>NA</td><td>8</td><td>73</td><td>104</td><td>U14, R45, U9</td></tr>
<tr><td colspan="5">*CW applicable only on exciter control and receiver-exciter control.</td></tr>
</table>
</td></tr>
<tr><td>11. Word 3, character 2 outputs

(Cont)</td><td>a. Strap mux control lines for word 3, character 2.

b. Apply logic 1 inputs at inputs associated with word 3, character 2 (see chart).

c. Apply logic 0 inputs at inputs associated with word 3, character 2 (see chart).</td><td>Note

Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. Word 3, character 2 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	112	26	U18, R103, U25
NA	2	47	28	U19, R97, R15
NA	3	113	29	U20, R91, U23
NA	4	48	94	U17, R86, U21
NA	5	107	30	U11, R81, U24
NA	6	*	31	U13, U16
NA	7	38	96	U12, U22
NA	8	103	104	U9, R42, U14

*Grounded input.

12. Word 3, character 3 outputs	a. Strap mux control lines for word 3, character 3.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 1.
	c. Apply logic 0 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 0.

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	42	26	U18, R104, U25
NA	2	108	28	U19, R98, U15
NA	3	43	29	U20, R92, U23
NA	4	109	94	U17, R87, U21
NA	5	44	30	U11, R82, U24
NA	6	110	31	U13, R78, U16
NA	7	111	96	U12, R75, U22
NA	8	46	104	U9, R72, U14

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>13. Word 3, character 4 outputs</td><td>a. Strap mux control lines for word 3, character 4.</td><td>Note
Grounded input as noted in chart will always be logic 0 output.
Verify that all associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>*</td><td>26</td><td>U18, U25</td></tr>
<tr><td>NA</td><td>2</td><td>*</td><td>28</td><td>U19, U15</td></tr>
<tr><td>NA</td><td>3</td><td>*</td><td>29</td><td>U20, U23</td></tr>
<tr><td>NA</td><td>4</td><td>*</td><td>94</td><td>U17, U21</td></tr>
<tr><td>NA</td><td>5</td><td>*</td><td>30</td><td>U11, U24</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U13, U16</td></tr>
<tr><td>NA</td><td>7</td><td>*</td><td>96</td><td>U12, U22</td></tr>
<tr><td>NA</td><td>8</td><td>*</td><td>104</td><td>U9, U14</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>14. Word 3, character 5 outputs

(Cont)</td><td>a. Strap mux control lines for word 3, character 5.

b. Apply logic 1 inputs at inputs associated with word 3, character 5 (see chart).

Note
PA PWR and P CAR switches apply logic 1 inputs in the positions indicated in the chart. In the OFF positions these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 3, character 5 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>14. Word 3, character 5 outputs (Cont)</td><td colspan="3">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>PA PWR-STBY</td><td>1</td><td>79</td><td>26</td><td>U18, R105, U25</td></tr>
<tr><td>PA PWR-HIGH PWR</td><td>2</td><td>14</td><td>28</td><td>U19, R99, U15</td></tr>
<tr><td>PA PWR-LOW PWR</td><td>3</td><td>78</td><td>29</td><td>U20, R93, U23</td></tr>
<tr><td>P CAR-ON</td><td>4</td><td>82</td><td>94</td><td>U17, R8, U21</td></tr>
<tr><td>NA</td><td>5</td><td>81</td><td>30</td><td>U11, R83, U24</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U13, U16</td></tr>
<tr><td>NA</td><td>7</td><td>*</td><td>96</td><td>U12, U22</td></tr>
<tr><td>NA</td><td>8</td><td>*</td><td>104</td><td>U9, U14</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>15. Word 4, character 2 outputs

(Cont)</td><td>a. Strap mux control lines for word 4, character 2.

b. Apply logic 1 inputs at inputs associated with word 4, character 2 (see chart).

Note

KEY switch in the LOCK position applies a logic 1 input and in the NORM position applies a logic 0 input.

c. Apply logic 0 inputs at inputs associated with word 4, character 2 (see chart).</td><td>Note

Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

15. Word 4, character 2 outputs (Cont)

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	*	26	U18, U25
NA	2	*	28	U19, U15
NA	3	*	29	U20, U23
NA	4	*	94	U17, U21
KEY-LOCK	5	68	30	U11, R12, U24
NA	6	*	31	U13, U16
NA	7	38	96	U12, U22
NA	8	103	104	U9, R42, U14

*Grounded input.

16. Word 4, character 3 outputs

a. Strap mux control lines for word 4, character 3.

b. Apply logic 1 inputs at inputs associated with word 4, character 3 (see chart). — Verify that associated outputs are at logic 1.

c. Apply logic 0 inputs at inputs associated with word 4, character 3 (see chart). — Verify that associated outputs are at logic 0.

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	18	26	U18, R106, U25
NA	2	101	28	U19, R100, U15
NA	3	39	29	U20, R94, U23
NA	4	83	94	U17, R88, U21
NA	5	36	30	U11, R84, U24
NA	6	105	31	U13, R79, U16
NA	7	40	96	U12, R76, U22
NA	8	2	104	U9, R73, U14

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>17. Word 4, character 4 outputs</td><td>a. Strap mux control lines for word 4, character 4.

b. Apply logic 1 inputs at inputs associated with word 4, character 4 (see chart).

c. Apply logic 0 inputs at inputs associated with word 4, character 4 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4"><table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>3</td><td>26</td><td>U18, R107, U25</td></tr>
<tr><td>NA</td><td>2</td><td>86</td><td>28</td><td>U19, R101, U15</td></tr>
<tr><td>NA</td><td>3</td><td>49</td><td>29</td><td>U20, R95, U23</td></tr>
<tr><td>NA</td><td>4</td><td>67</td><td>94</td><td>U17, R89, U21</td></tr>
<tr><td>NA</td><td>5</td><td>70</td><td>30</td><td>U11, R85, U24</td></tr>
<tr><td>NA</td><td>6</td><td>5</td><td>31</td><td>U13, R80, U16</td></tr>
<tr><td>NA</td><td>7</td><td>4</td><td>96</td><td>U12, R77, U22</td></tr>
<tr><td>NA</td><td>8</td><td>69</td><td>104</td><td>U9, R74, U14</td></tr>
</table></td></tr>
<tr><td>18. Word 4, character 5 outputs

(Cont)</td><td>a. Strap mux control lines for word 4, character 5.

b. Apply logic 1 inputs at inputs associated with word 4, character 5 (see chart).

c. Apply logic 0 inputs at inputs associated with word 4, character 5 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
18. Word 4, character 5 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	80	26	U18, R108, U25
NA	2	16	28	U19, R102, CR24, C28, U15
NA	3	95	29	U20, R96, U23
NA	4	71	94	U17, R90, U21
NA	5	*	30	U11, U24
NA	6	*	31	U13, U16
NA	7	*	96	U12, U22
NA	8	*	104	U9, U14
*Grounded input.				

4. REPAIR

Repair of the parallel input card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

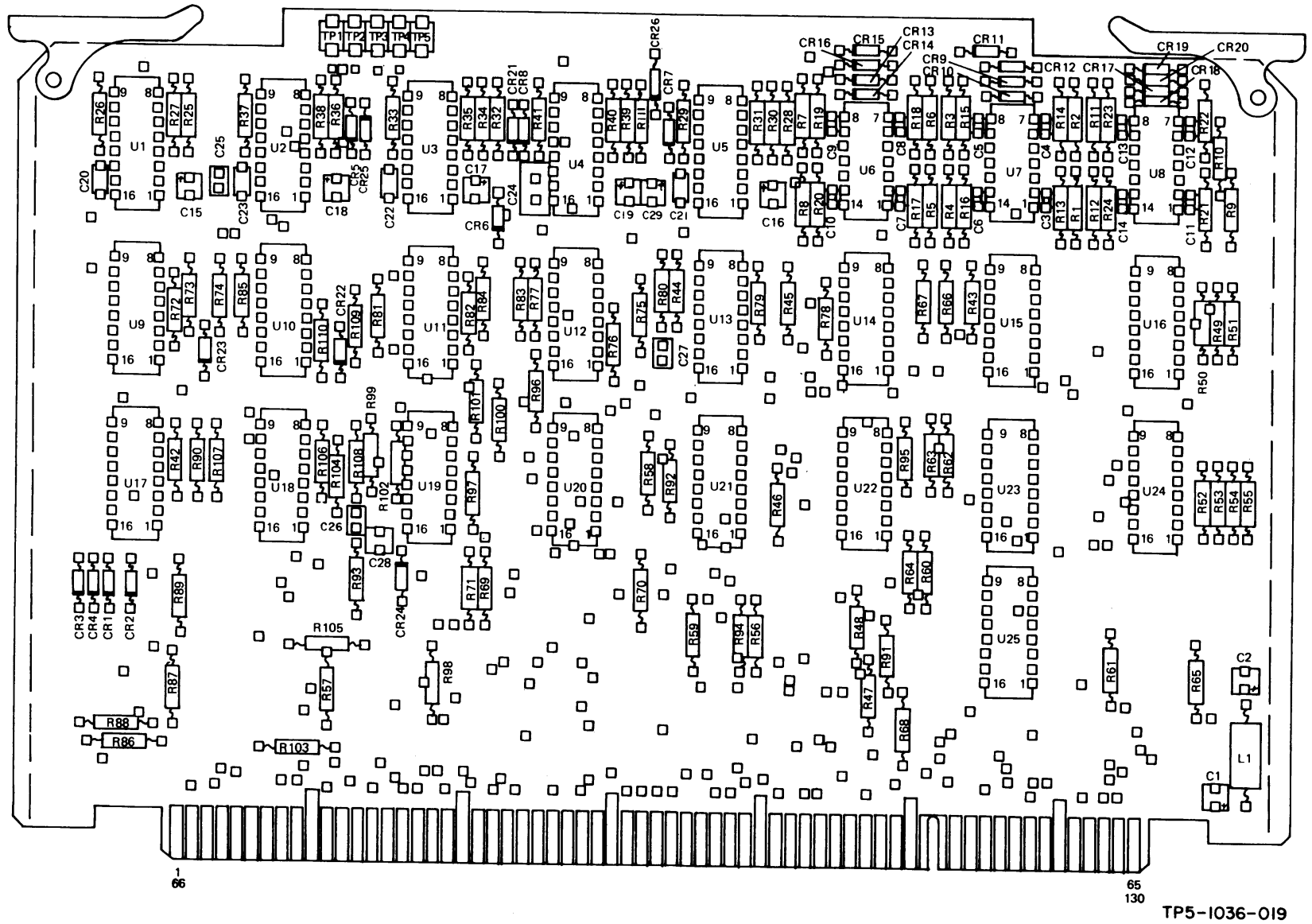
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 4. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel input	635-0751-001	REV N
Parallel input	635-0751-002	REV M



TP5-1036-019

Parallel Input, Schematic Diagram
Figure 4 (Sheet 1 of 8)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	PARALLEL INPUT 635-0751-001		A
	PARALLEL INPUT 635-0751-002		B
CR1-CR24	SEMICOND DEVICE, 1N4454	353-3644-010	
CR25, CR26	SEMICOND DEVICE, 1N4454 (A4)	353-3644-010	A
C1, C2	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C3-C14	CAPACITOR, FXD, CER DIEL, 1000pF, 20%, 50V	913-3279-030	
C15	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V (A1)	184-9102-390	A
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	A
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	B
C16-C19	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C20-C23	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C24	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C25-C27	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C28	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V (A2)	184-9102-350	A
C28	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V	184-9102-390	A
C28	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V	184-9102-390	B
C29	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V (A3)	184-9102-390	A
C29	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-390	B
L1	COIL, RF, 1000μH	240-2540-000	
R1-R12	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R13-R25	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R26	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R27, R28	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R29	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R30-R32	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R33	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R34-R36	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R37	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R38-R40	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R41	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R42-R108	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R109	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R110	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R111	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W (A3)	745-0857-000	A
R111	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	B
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
U1-U5	INTEGRATED CKT, MC14528BCP	351-8421-020	
U6-U8	INTEGRATED CKT, F4030BPC	351-8159-190	
U9	INTEGRATED CKT, MC14512CP	351-8420-020	
U10	INTEGRATED CKT, F4049BPC	351-8159-210	
U11-U25	INTEGRATED CKT, MC14512CP	351-8420-020	

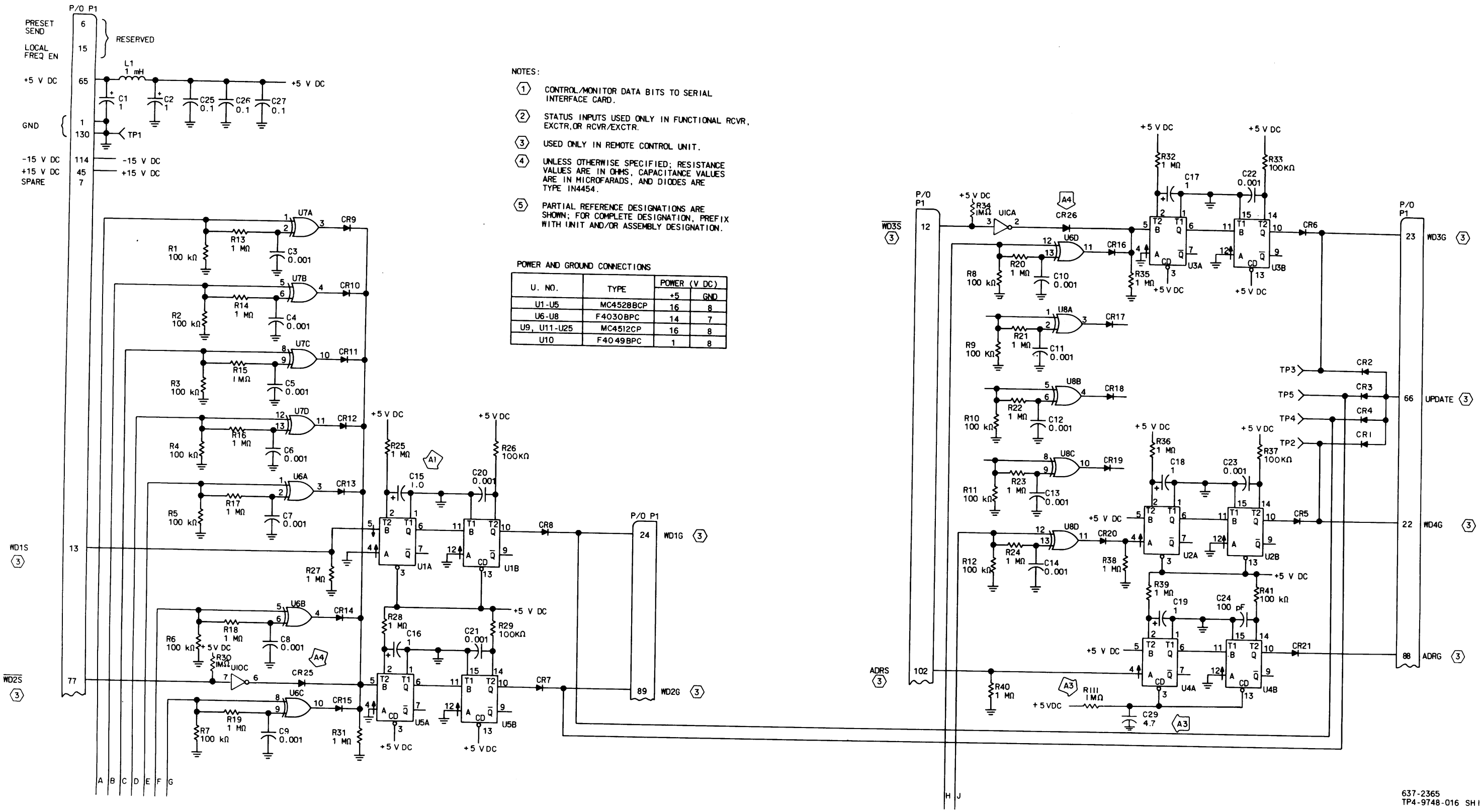
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed C15 fron 4.7μF to 1.0 μF.	REV C and above
A2	Changed C28 from 1.0μF to 4.7μF.	REV D and above
A3	Added R111, 1MΩ and C29, 4.7μF.	REV E and above
A4	Added CR25, 1N4454 and CR26, 1N4454.	635-0751-001, REV K and above

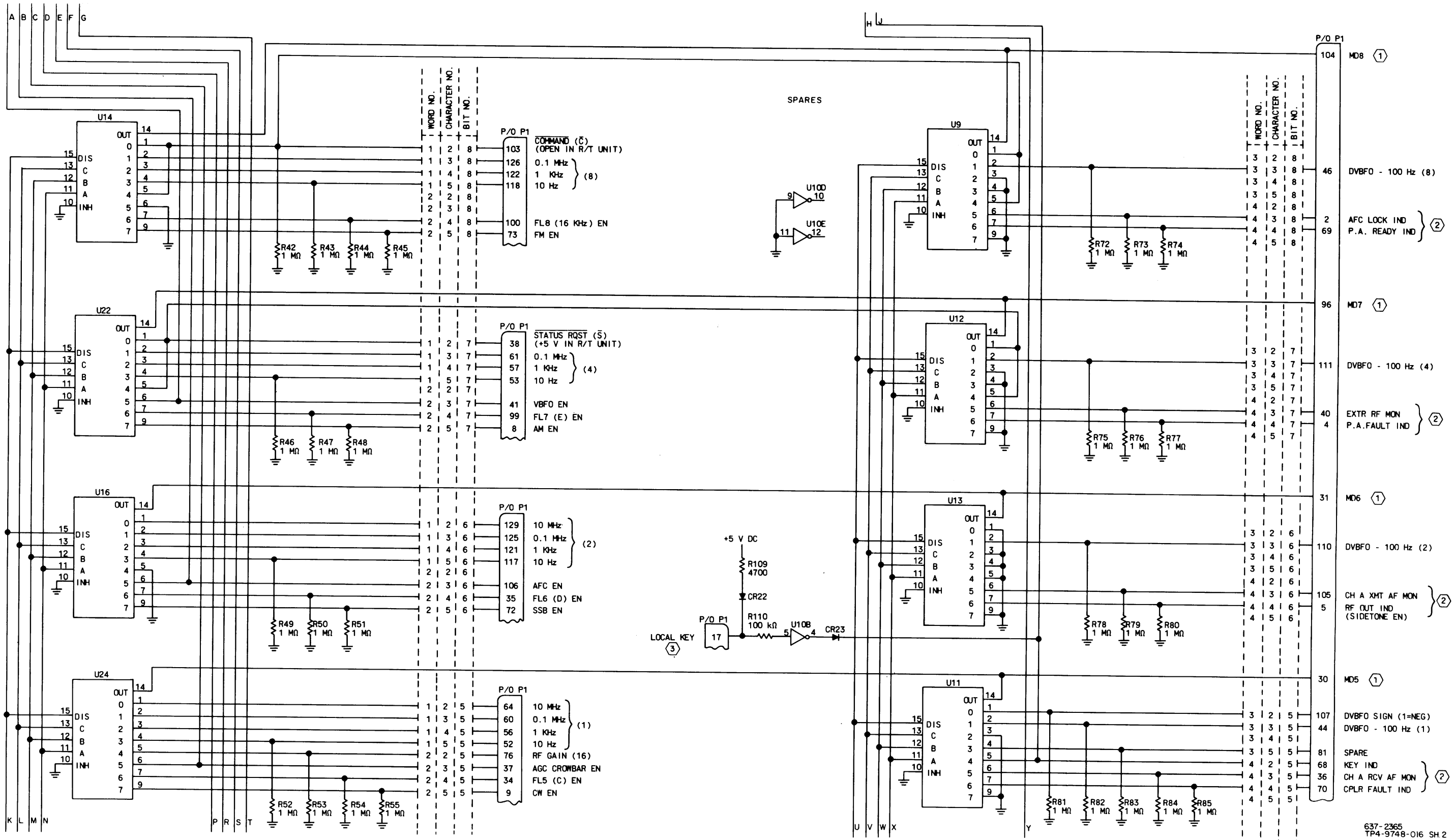
Note

The preceding modification history effectivities apply only to the 635-0751-001. Preceding modifications are included in all 635-0751-002 cards.

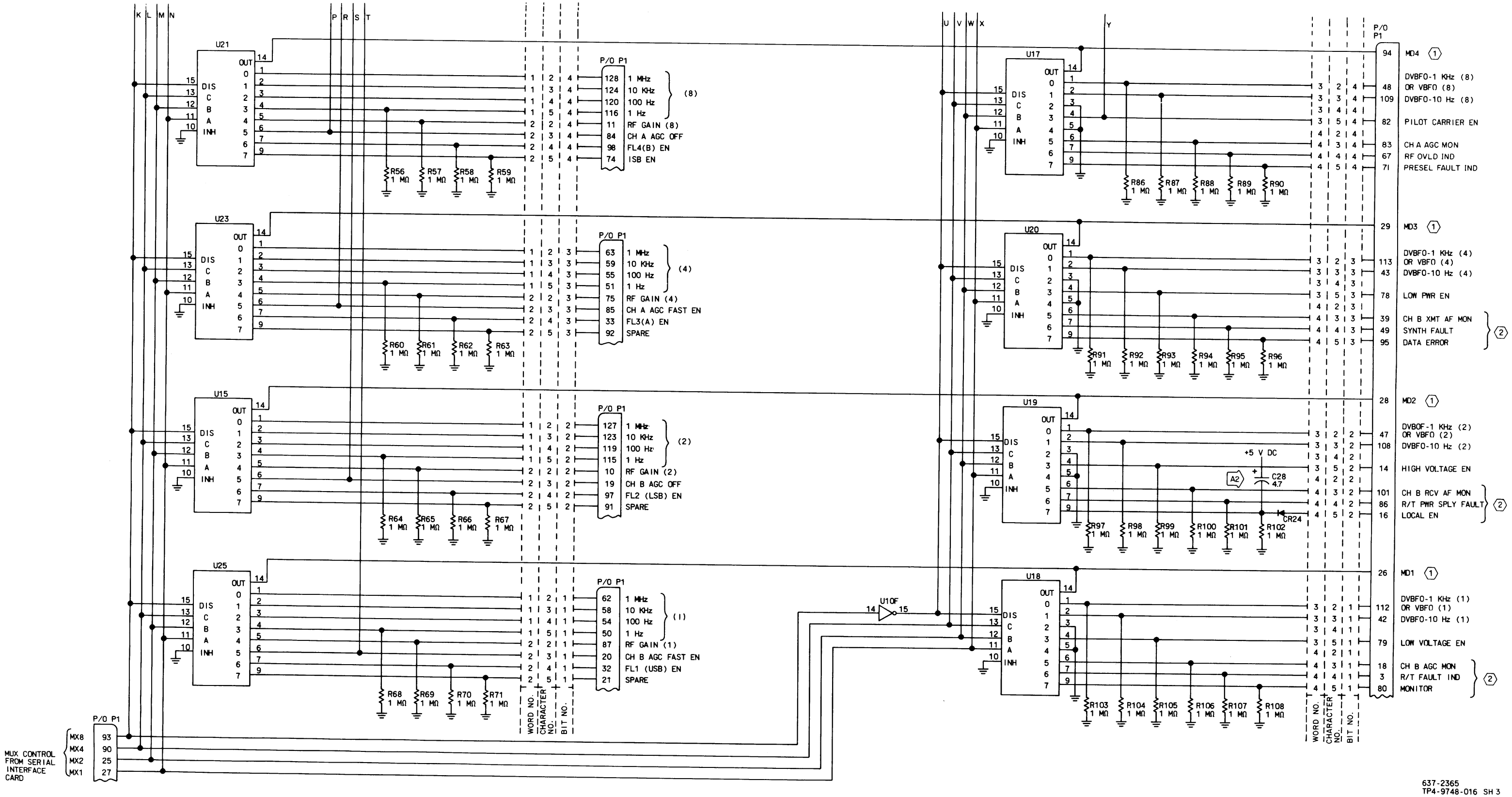
Parallel Input, Schematic Diagram
Figure 4 (Sheet 2)



Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 3)



Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 4)

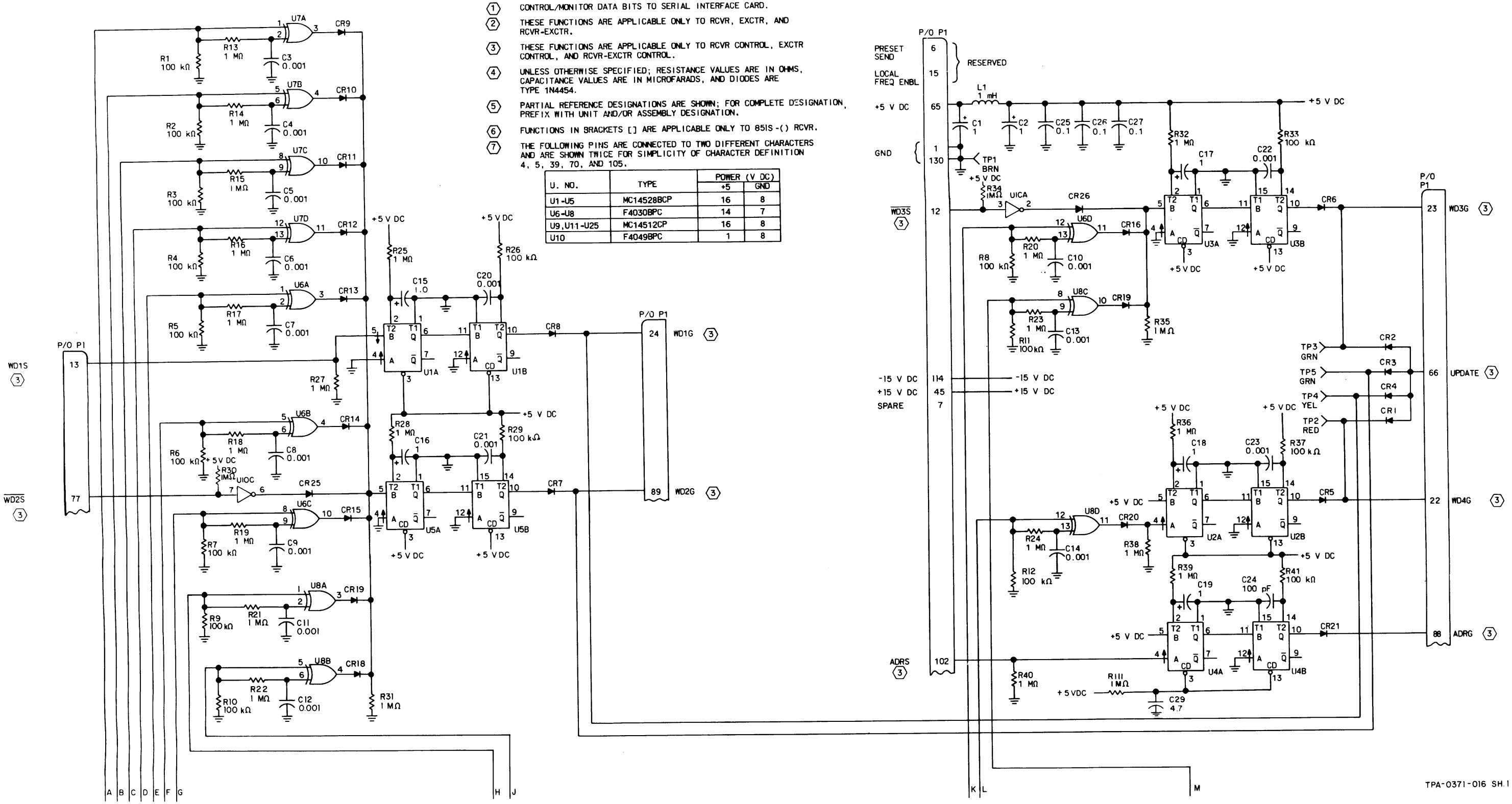


Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 5)

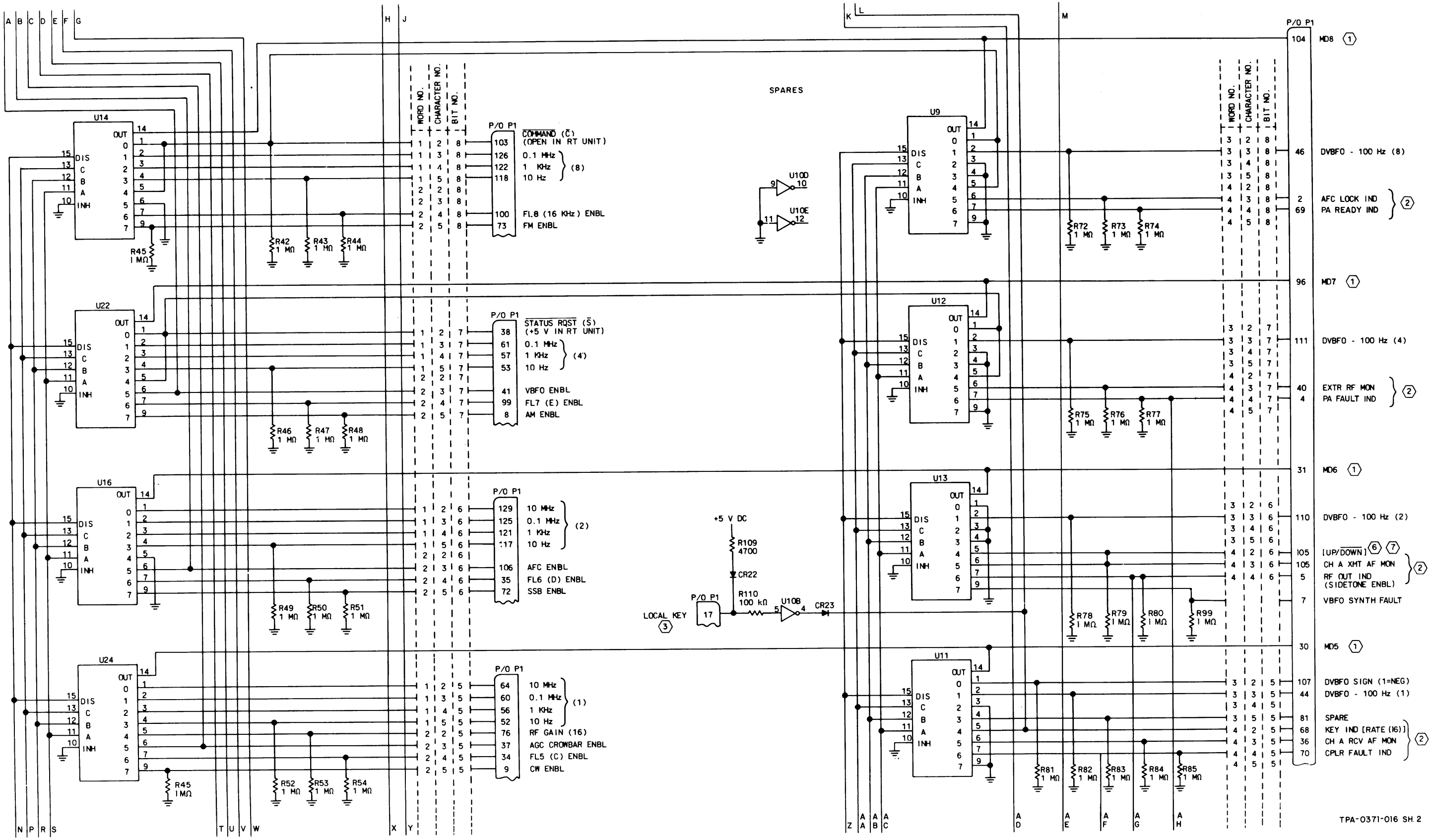
NOTES:

1. CONTROL/MONITOR DATA BITS TO SERIAL INTERFACE CARD.
2. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR, EXCTR, AND RCVR-EXCTR.
3. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR CONTROL, EXCTR CONTROL, AND RCVR-EXCTR CONTROL.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
6. FUNCTIONS IN BRACKETS [] ARE APPLICABLE ONLY TO 8515-() RCVR.
7. THE FOLLOWING PINS ARE CONNECTED TO TWO DIFFERENT CHARACTERS AND ARE SHOWN TWICE FOR SIMPLICITY OF CHARACTER DEFINITION 4, 5, 39, 70, AND 105.

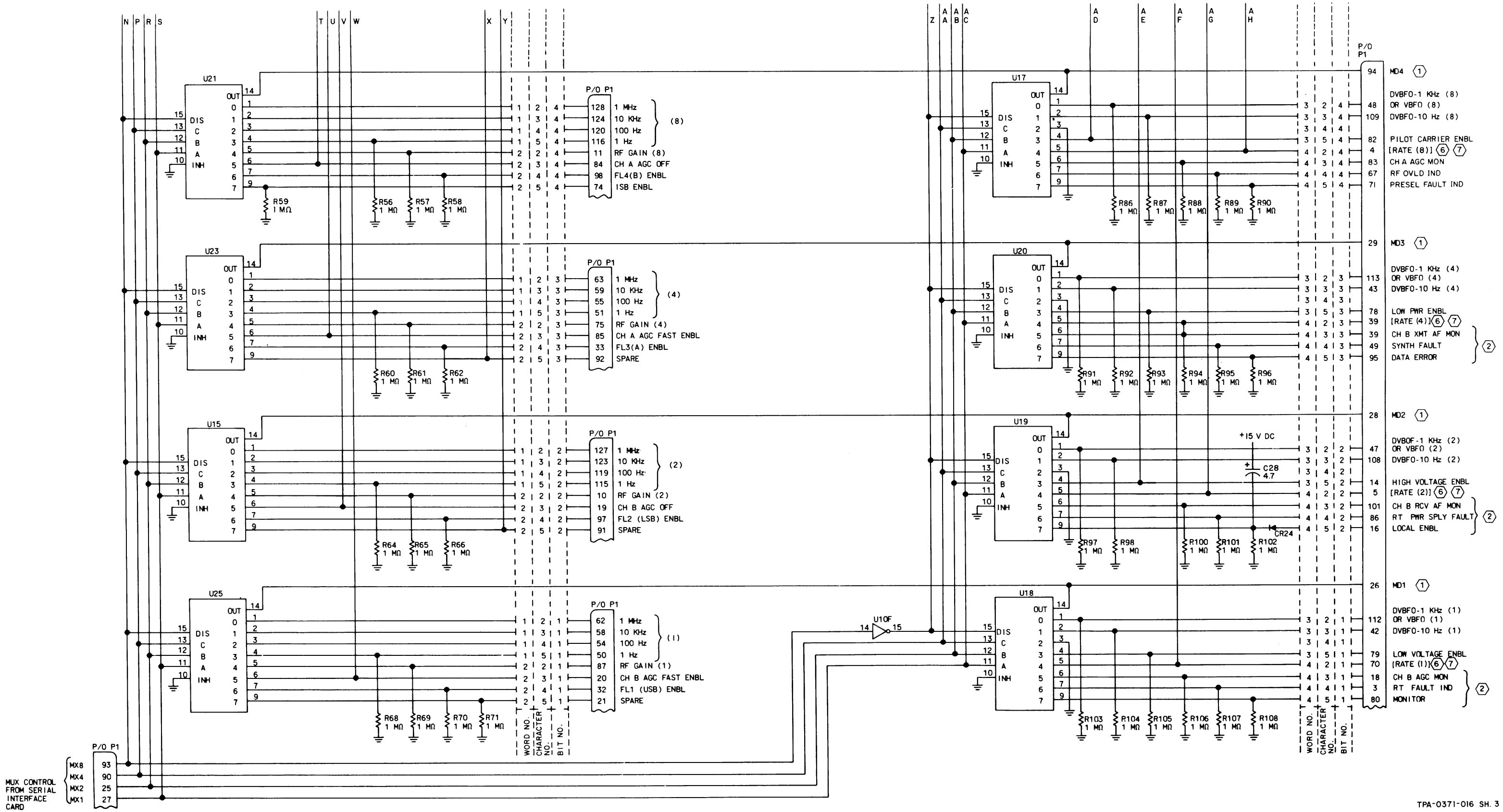
U. NO.	TYPE	POWER (V DC)	
		+5	GND
U1-U5	MC14528BCP	16	8
U6-U8	F4030BPC	14	7
U9,U11-U25	MC14512CP	16	8
U10	F4049BPC	1	8



Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 6)



Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 7)



TPA-0371-016 SH. 3

Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 8)